112 Gbit/s Single-Polarization Silicon Coherent Receiver with Hybrid-Integrated BiCMOS Linear TIA

Jochem Verbist[(1),(2)], Jing Zhang[(2)], Bart Moeneclaey[(1)], John van Weerdenburg[(3)], Roy van Uden[(3)], Chigo Okonkwo[(3)], Xin Yin[(1)], Johan Bauwelinck[(1)], Gunther Roelkens[(2)]

[(1)] INTEC design, Ghent University - iMinds - IMEC, Sint-Pietersnieuwstraat 41, 9000 Ghent, Belgium, Jochem.Verbist@intec.ugent.be
[(2)] Photonics Research Group, Ghent University - IMEC, 9000 Ghent, Belgium
[(3)] COBRA Research Institute, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands

Abstract *We report the design, fabrication and verification of a single-polarization silicon coherent receiver with a low-power linear TIA array. Error-free operation assuming FEC is shown at bitrates of 112 Gbit/s (28 Gbaud 16-QAM) and 56 Gbit/s (28 Gbaud QPSK).*

Introduction

Coherent communication allows increasing the spectral efficiency of optical communication networks and is therefore of great interest in order to accommodate the ever increasing need for bandwidth. This evolution took place first in the long-haul communication networks, but is now also penetrating into the metro and access network domain. Implementing coherent communication in shorter reach networks requires decreasing the cost, footprint and power consumption of coherent transceivers. Silicon photonics is emerging as an attractive platform to realize such transceivers on, given the possibility for large volume fabrication at low cost and small footprint of the resulting devices[1-3].

In this paper we report on the realization of a 28 Gbaud silicon coherent receiver with hybrid integrated low-power linear transimpedance amplifier array supporting single polarization QPSK and 16-QAM. The silicon photonic coherent receiver was realized in imec's iSIPP25G silicon photonics platform, while 0.13µm SiGe BiCMOS technology was used for the transimpedance amplifiers. A hybrid integration approach is preferred over a monolithic approach as it allows independent optimization of the used technology for the photonics and electronics, reducing the cost and allowing commercial silicon foundry services to be used.

Receiver Design

A microscope image of the hybrid-integrated receiver on a printed circuit board is shown in Fig. 1a. Care was taken during assembly of placing the TIA die (3mm x 0.9mm) and the silicon photonic integrated circuit (PIC, 0.3mm x 0.5mm) as close together as possible to minimize lengths of the interconnecting wirebonds. The silicon

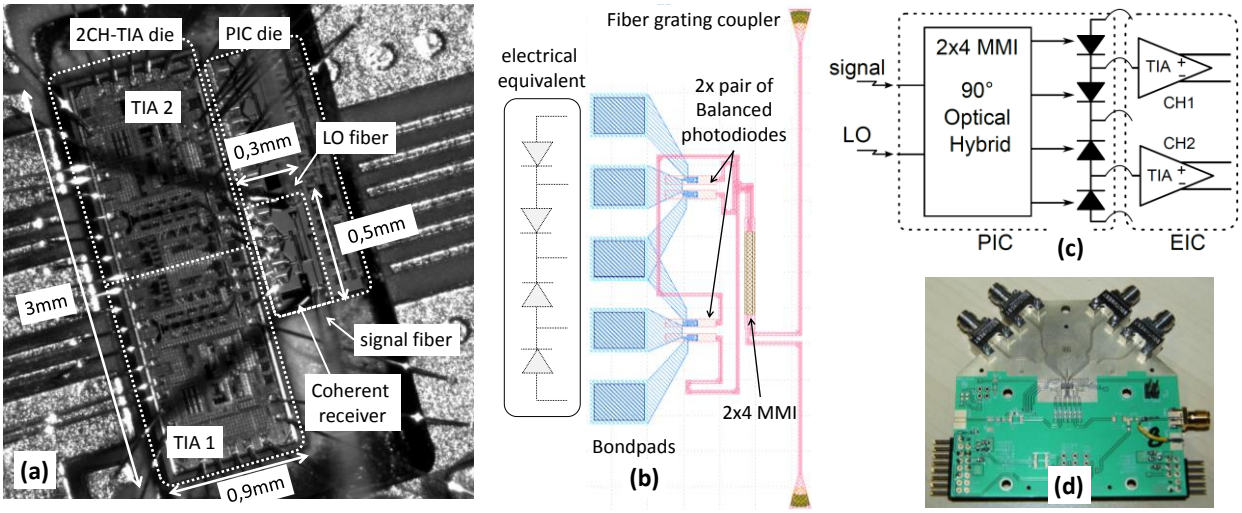

Fig. 1: close-up of wirebonded electronic and photonic die on the PCB (**a**); optical design of coherent detector (**b**); schematic of coherent receiver (**c**); PCB assembly (**d**)

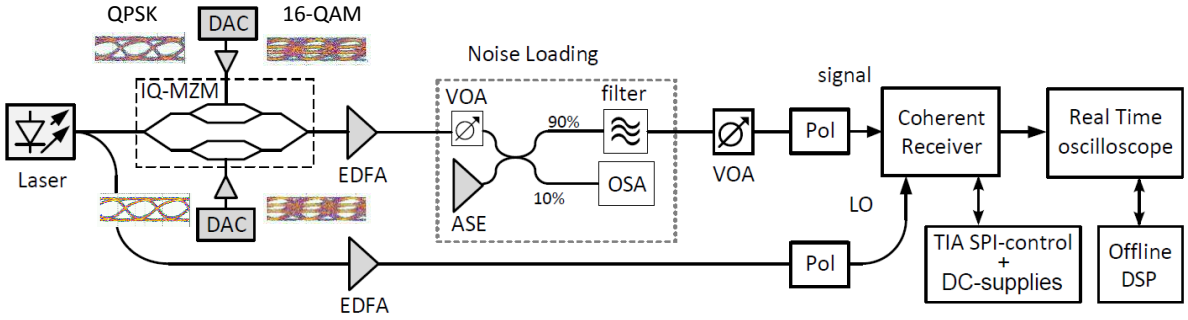

Fig. 2: Schematic of characterization setup of the receiver (i.e. the PCB with the photonic and electronic die), for QPSK and 16-QAM modulation

photonic coherent receiver (Fig. 1b) uses 1D grating couplers (6.5dB insertion loss) to couple the signal and local oscillator quasi-vertically into the PIC. These inputs are then combined in a 2x4 multimode interferometer 90° optical hybrid resulting in an I, Q, -I, -Q output[4]. These signals are detected by 2 pairs of balanced germanium photodiodes (Fig. 1 top right). The germanium photodiodes have a 3dB-bandwith of 50 GHz and a responsivity of ~0.5 A/W. The use of balanced diodes boosts the sensitivity by 3dB and cancels the RIN of the laser sources.

The output current of the optical receiver is amplified by a 2-channel-TIA array fabricated in a 0.13µm SiGe BiCMOS process. The chip was designed and tested for linear operation in a PAM-4 receiver for data rates up to 32 Gbaud[5]. The linear behaviour makes it ideally suited for high-speed 16-QAM modulation as both TIA channels actually receiver a PAM-4 signal (respectively the I- and Q-modulated components of the data).

To enable easy measurements and control of TIA settings a 4-layer PCB was designed as shown in Fig. 1d. Both dies were placed in a cavity in the centre of the PCB as to minimize the height gap (and by this the length) of the wirebonds between TIA and the traces on the PCB. The 2x2 differential outputs of the 2CH-TIA were routed symmetrically to 4 high speed connectors at the edge of the board. Due to the limitations of the setup in our lab all measurements were done single-ended by terminating the corresponding output of the differential signal with a DC-block and a 50Ω resistor. The PCB wasn't minimized in size (apart from the differential output traces to the screw-on high-speed connectors) as to enable easy testing and assembly.

Characterization setup

The coherent receiver was evaluated at 28 Gbaud. At the transmitter side the light of a C-band external cavity laser operating at 1550.92 nm is split in two parts: one for the LO and one for the signal. The signal part is guided through a $LiNbO_3$ Mach-Zehnder IQ-modulator (IQ-MZM) where it's modulated with a 2^{15}-1 long PRBS signal at 28 Gbaud and amplified by an EDFA. The IQ-MZM is driven by 2 DACs: one generating the in-phase and the other one the quadrature part of the constellation, i.e. QPSK (2 bits/symbol) or 16-QAM (4 bits/symbol). The DACs also present a speed bottleneck in the setup as they are limited to 32 GS/s (and operated at 28 GS/s). In principal our receiver should be able to support 40 Gbaud operation[5,6]. For OSNR measurements amplified spontaneous emission (ASE) noise is added to the modulated signal in a noise loading stage. A variable optical attenuator provides the desired signal power to the receiver.

The other part of the laser light is amplified by a second EDFA and serves as the LO for the coherent receiver. Polarization controllers allow efficient coupling of TE polarized light into the silicon photonic receiver. The light from these two fibers is coupled under an angle of ~17° w.r.t. the vertical into the photonic die by 1D-grating couplers.

The output of the TIA is read out by a 50 GHz 160 GS/s real-time oscilloscope and post-processed offline by DSP software. The characterization setup is shown in Fig. 2.

Measurement results and discussion

Initial measurements focused on 28 Gbaud single polarization QPSK (56 Gbit/s), using 12 dBm fiber coupled LO power (~5 dBm on-chip). The transimpedance of the TIA was tuned to achieve optimal BER performance for the given data rate (28 Gbaud) by trading off a lower gain for a higher bandwidth. The reverse bias for balanced photodiodes was set though the TIA. The transmission is below the FEC-limit (i.e. 3.8×10^{-3} at 7% overhead) for an OSNR of 12dB. The OSNR penalty w.r.t. the theoretical optimum at the FEC-limit is less than 2.5dB. The bit error rate versus OSNR is plotted in Fig. 3a, together with two representative constellation diagrams. During the QPSK measurements we sporadically saw phase rotations in the received constellation. Research is being conducted to the cause of these fluctuation. A possible cause is

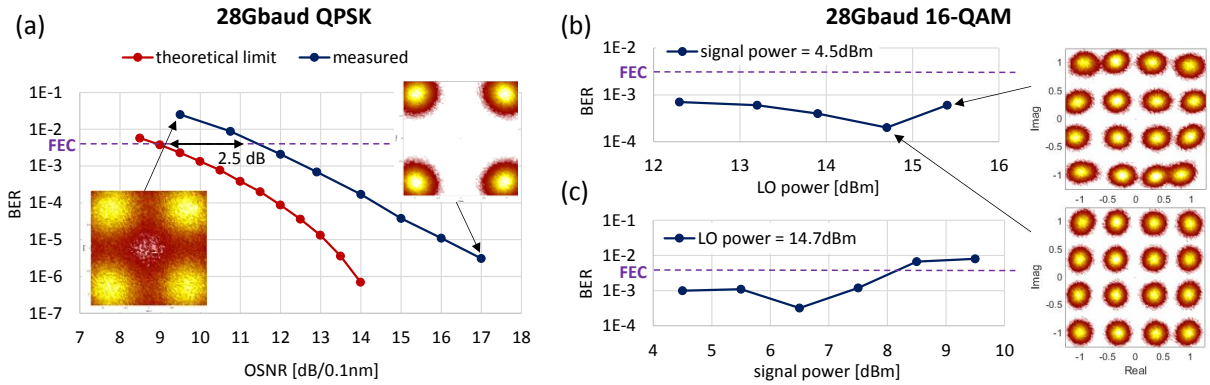

Fig. 3: BER vs OSNR curve for 28Gbaud QPSK, the noise was added starting form signal power of -2.5 dBm and LO power of -2.3 dBm (**a**); BER vs input power for 28 Gbaud 16-QAM with varying LO power (**b**) and varying signal power (**c**)

the non-stable mechanical setup of the fiber alignment where slight vibrations could already cause significant phase rotations due to the difference in optical path length. A new setup is being prepared to deal with this issue. Due to the more stringent phase and amplitude tolerances for 16-QAM our setup is being limited by the performance of the DACs on the transmitter side. The minimal obtainable BER for this constellation by a commercial coherent receiver, used as bench mark for the system, saturated around $2x10^{-5}$. This behaviour in combination with the erratic phase fluctuations prevented us from achieving a stable and low enough BER for a meaningful OSNR measurement.

So for 16-QAM we present BER vs input power measurements, where we swept the LO power for a constant signal power (4.5 dBm) (Fig. 3b) and the signal power for a constant LO-power (14.7 dBm) (Fig 3c). The receiver remains below FEC over a range of ~4 dB. In both curves the error rate increases again after a certain input power, indicating possible degeneration of the transimpedance amplifier or saturation of the photodiodes due to the high input power.

The 2 channel TIA array pulls a total current of 128 mA (at the highest signal and LO power), yielding a low overall power consumption of 310mW or 2.8 mW/Gbit/s for 16-QAM transmission (and 5.8 mW for QPSK) in agreement with other work[7-9].

Conclusions

We successfully demonstrated a silicon coherent receiver realized in IMEC's silicon photonics platform co-integrated with a 0.13µm BiCMOS linear TIA for 28 Gbaud QPSK and 16-QAM in a single polarization. The overall power consumption of device is less than 310 mW resulting in a low 2.8 mW/Gbit/s for 16-QAM. The receiver will be further characterized for data rates up to 40 Gbaud with the aid of faster DACs. Hybrid integration of photonic and electronic die could provide a flexible and cost-effective path for silicon photonics for achieving low-cost, high-speed transmission systems.

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